**WE CLAIM:**

1. An integrated semiconductor circuit, comprising:

a cell array, the cell array having a plurality of memory cells, each memeory cell having a selection transistor and a storage capacitor andcapable of being driven electrically by bit lines and word lines;

the storage capacitors, the bit lines, and the word lines being arranged in different planes on or in a semiconductor substrate;

a plurality of electrical contact structures, the electrical contact structures being arranged at the level of the word lines, the contact structures electrically connecting the bit lines to the selection transistors of the memory cells,

the contact structures leading past the word lines and being insulated from the word lines by lateral insulations; and

in each case, at least two bit lines being connected to a common signal amplifier,

wherein at least one first and a second additional word line are provided, which cannot be used for driving selection transistors, each bit line extending as far as the first or second additional word line and is connected to an additional contact structure, the additional contact structure leading which leads laterally past one of the two additional word lines and representing a dummy contact, additional contact structures of two bit lines leading past different additional word lines, in each case, the two bit lines being connected to the same signal amplifier.

2. The semiconductor circuit as claimed in claim 1, wherein two mutually adjacent bit lines in each case are connected to the same signal amplifier.

3. The semiconductor circuit as claimed in claim 1, wherein the additional contact structures of mutually nearest adjacent bit lines alternately lead past the first additional word line and the second additional word line.

4. The semiconductor circuit as claimed in claim 1, wherein each of the two additional word lines can be activated jointly with an arbitrary word line past which lead contact structures exclusively of those bit lines which do not have an additional contact structure leading past the respective additional word line.

5. The semiconductor circuit as claimed in claim 1, wherein the storage capacitors are trench capacitors arranged in the semiconductor substrate, and the bit lines are arranged on the semiconductor substrate at a greater distance from the semiconductor substrate than the word lines.

6. The semiconductor circuit as claimed in claim 1, wherein the additional contact structures which lead past the additional word lines end on a trench isolation of the semiconductor substrate, whereas the contact structures of the remaining word lines in each case lead into a common doping region of two selection transistors.

7. The semiconductor circuit as claimed in claim 1, wherein the first and the second additional word line are arranged beside one another at an edge of the cell array.

8. The semiconductor circuit as claimed in claim 1, wherein the selection transistors are field-effect transistors, the gate electrodes of the field-effect selection transistors being formed by the word lines.

9. The semiconductor circuit as claimed in claim 1, wherein the lateral insulations between the contact structures and the word lines are sidewall coverings of patterned gate layer stacks.

10. The semiconductor circuit as claimed in claim 1, wherein the semiconductor circuit is a dynamic random access memory.